

CT μ L-952 THROUGH CT μ L-957

FAIRCHILD PLANAR EPITAXIAL COMPLEMENTARY TRANSISTOR MICROLOGIC

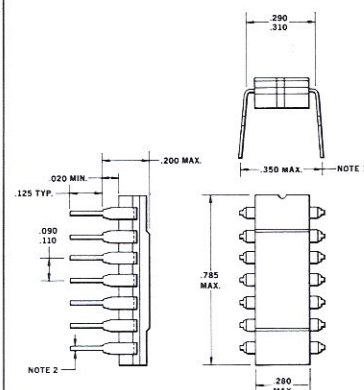
GENERAL DESCRIPTION - The Fairchild CT μ L Family was designed for very high-speed, low-cost commercial systems applications. It features AND - OR - NOT logic.

Using CT μ L, the system designer can obtain average propagation delays per logic decision of 5 ns, with associated rise times of 5 to 15 ns. Binary counting rates of 30 MHz are typical. Special circuit design techniques have been used on DT μ L to permit open transmission lines of 12-15 inches and still keep operation in the 5 ns speed range. Logic swings are typically 3 volts. Noise margins are typically 0.5 volt or greater.

The system designer may use proven, low-cost, system fabrication techniques including two-sided printed circuit boards, simplified manual or automated insertion, flow-soldering attachment, "functional" printed circuit board layout and simple system heat removal schemes.

CT μ L circuits are packaged in a ceramic package having short stiff leads in a dual in-line arrangement. CT μ L circuits are designed to operate over a commercial ambient temperature range of +15 to +55°C. Power supplies are +4.5 V $\pm$ 10% and -2 V $\pm$ 10%. Power dissipation was designed to increase with fan-in and fan-out. Inverter Gates or AND Gates dissipate 30 to 35 mW nominally plus 5 mW per fan-out.

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

THE COMPLEMENTARY TRANSISTOR MICROLOGIC FAMILY:

CT μ L-952 —Dual 2-Input Inverter Gate (two circuits in one package). This element is used mainly for voltage level setting and logic inversion. Its high level output is regulated for voltage and temperature to track the input "turn-on" threshold of other inverter gates. The output may be tied to any other output in the CT μ L family to perform the OR function. Average propagation delay is typically 9 to 12 ns.

CT μ L-953 —2-2-3-Input AND Gate (three gates in one package).

CT μ L-954 —Dual 4-Input AND Gate (two gates in one package).

CT μ L-955 —8-Input AND Gate with two outputs. The AND Gates (953, 954, 955) are non-inverting, non-saturating, PNP-NPN, cascade-connected emitter-followers. The 955 element has two separate outputs that may be used to isolate the output logic signal. Any AND Gate output may be OR tied to any other outputs in the CT μ L family. Average propagation delay of the AND Gates is 2.7 to 4 ns, depending on loading.

CT μ L-956 —Dual 2-Input Buffer (two buffers in one package). The Buffer is a non-inverting, level setting circuit intended to drive high fan-outs. It may also be used as a line-driver. Average propagation delay is typically 12 to 15 ns.

CT μ L-957 —Dual-Rank Flip-Flop. This is a multi-purpose, directly-coupled, dual-rank flip-flop useful for counters, registers and other "storage" applications. Outputs of the 957 provide voltage levels identical to the 952 Inverter Gate Output. Through delay from the blocking inputs going negative to ① the output going positive is typically 15 ns and ② the other output going negative, is 20 ns. Minimum data input pulse width is typically 12 ns.

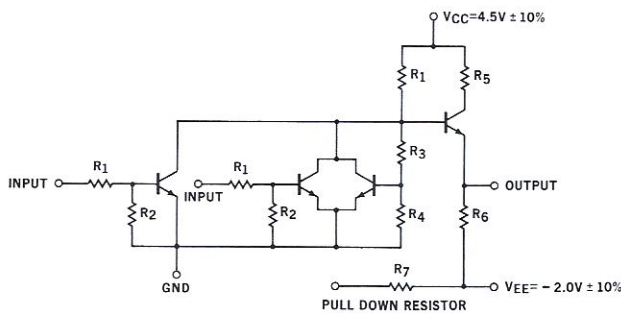
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FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC

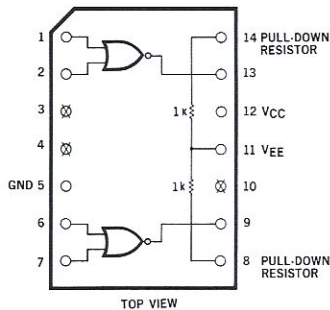
CT μ L-952 DUAL 2-INPUT INVERTER GATE

CIRCUIT DIAGRAM



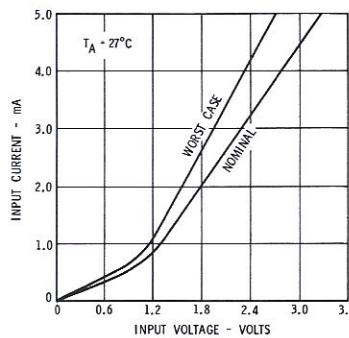
NOTE: ONLY ONE 2-INPUT INVERTER GATE SHOWN

LOGIC DIAGRAM (POSITIVE LOGIC)

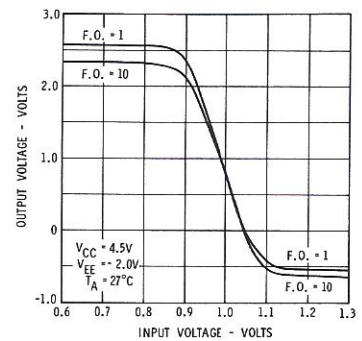


TOP VIEW

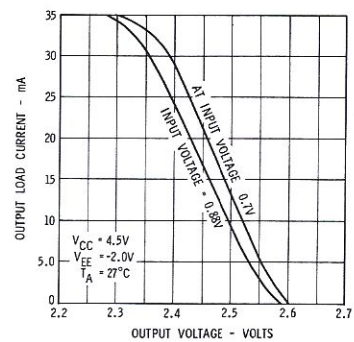
INPUT CHARACTERISTICS



TYPICAL TRANSFER CHARACTERISTICS

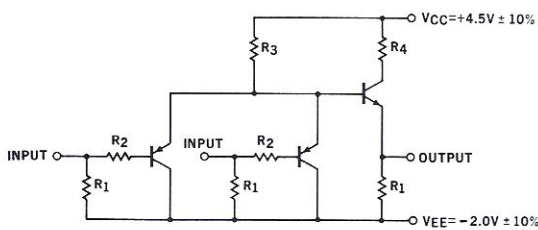


TYPICAL HIGH-LEVEL OUTPUT CHARACTERISTICS



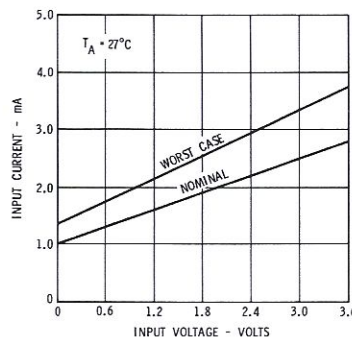
CT μ L-953, 954, 955 AND GATES

TYPICAL CIRCUIT DIAGRAM

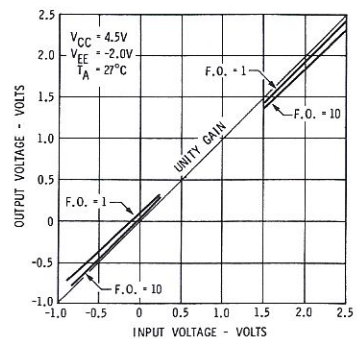


NOTE: ONLY ONE 2-INPUT GATE SHOWN

INPUT CHARACTERISTICS

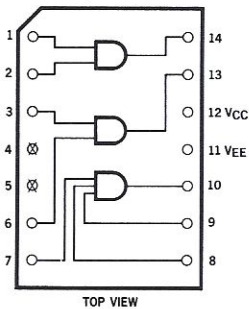


TYPICAL TRANSFER CHARACTERISTICS



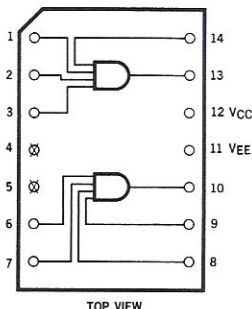
LOGIC DIAGRAMS (POSITIVE LOGIC)

CT μ L-953



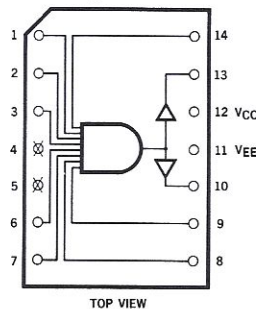
TOP VIEW

CT μ L-954



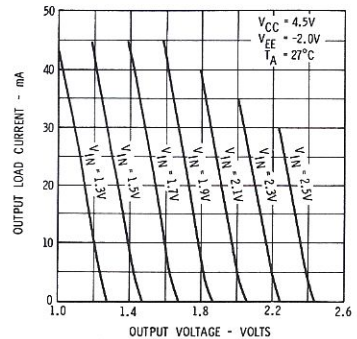
TOP VIEW

CT μ L-955



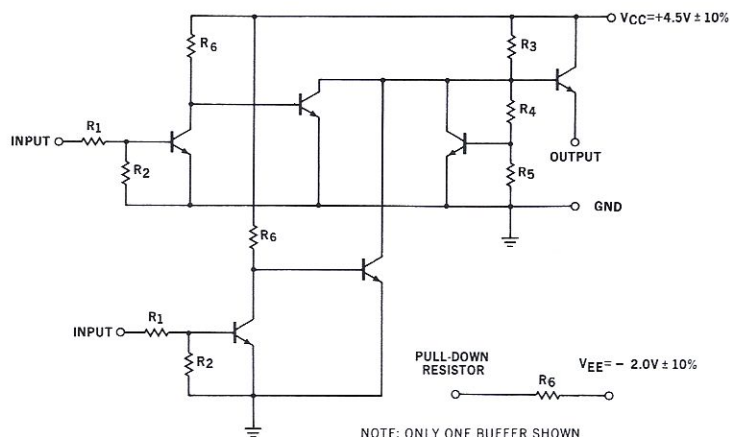
TOP VIEW

TYPICAL OUTPUT CHARACTERISTICS

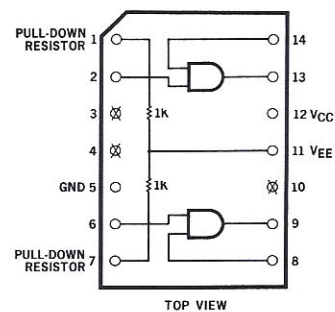


FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC

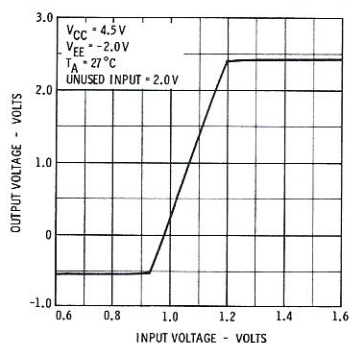
CT μ L-956 BUFFER CIRCUIT DIAGRAM



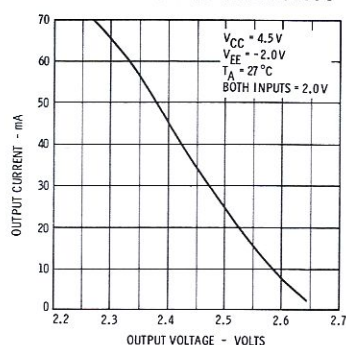
CT μ L-956 LOGIC DIAGRAM
(POSITIVE LOGIC)



CT μ L-956 TYPICAL
TRANSFER CHARACTERISTICS

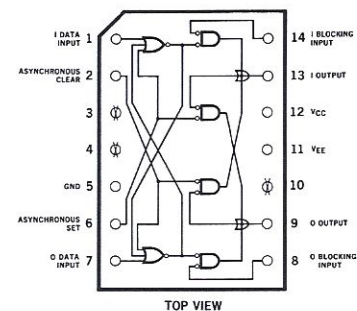


CT μ L-956 TYPICAL HIGH-LEVEL
OUTPUT CHARACTERISTICS

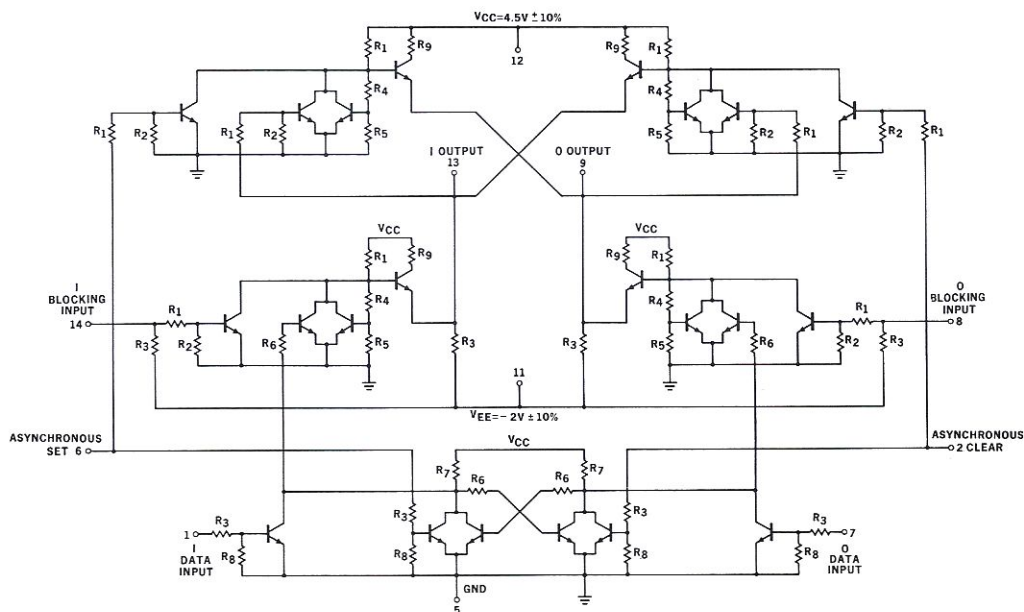


(INPUT CHARACTERISTICS SAME AS CT μ L-952)

CT μ L-957 LOGIC DIAGRAM
(POSITIVE LOGIC)



CT μ L-957 DUAL-RANK FLIP-FLOP CIRCUIT DIAGRAM



NOTE: $\emptyset$ = PIN NOT USED

FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC

AND-OR LOGIC: Greatest system speed will be realized by performing most of the logic with the AND Gates ("AND"ing with the inputs, "OR"ing with the outputs). After several levels of this, the slower Inverters or Buffers may be used to re-establish noise immunity levels.

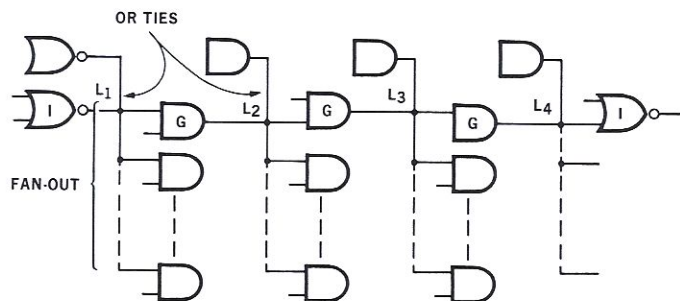
CT_μL NORMALIZED LOADING CHART

ELEMENT	INPUT	MAX. OUTPUT
952	1.5	12
953	1	15
954	1	15
955	1	Sum of both outputs = 15
956	1.5	25 (or for 50Ω line: 68Ω to GND with F.O. = 10 AND gates)

ELEMENT	DATA INPUT	BLOCKING GATE INPUT	ASYNCHRONOUS INPUT	OUTPUT
957	1	3.5	2	9.5

LEVEL RESETTING: There is signal level degradation going through an AND Gate; therefore, signal level must be restored after going through several cascaded gates. This may be accomplished by using either the 952 Inverter Gate, the 956 Buffer, or by driving the 957 Flip-Flop. The purpose of the following loading rules is to guarantee a worst case noise immunity at L_4 of 250 mV.

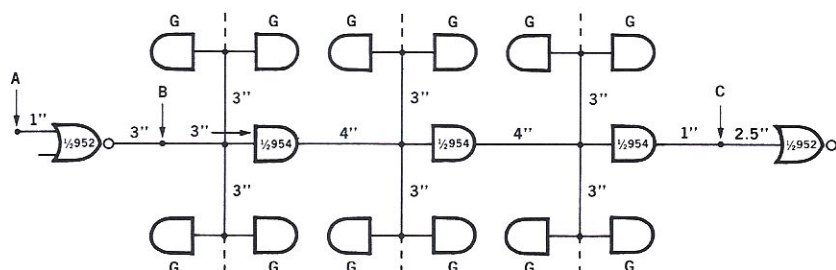
LOADING RULES: For the case of Three Cascaded AND Gate Levels



NOTES:

1. Loads and OR Ties at $L_1 + L_2 + L_3 + L_4 \leq 45$.
2. Maximum Loading at $L_1 = 12$, $L_2 = 15$, $L_3 = 15$, $L_4 = 15$.
3. Both Rules 1 and 2 Must be Satisfied Simultaneously.

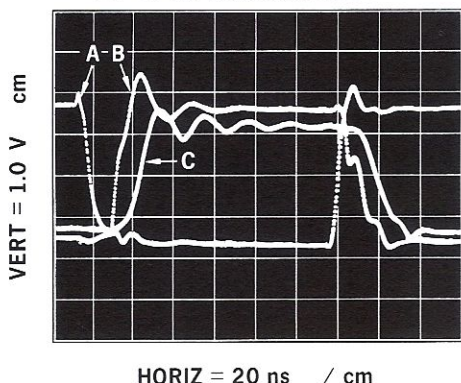
PROPAGATION DELAY TEST SET-UP



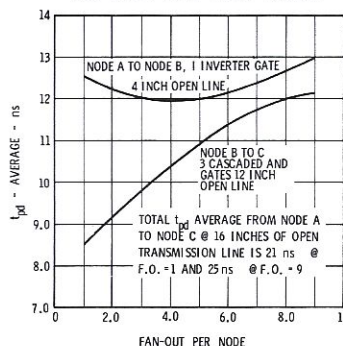
NOTES:

1. Above configuration may have as many as 8 logic levels for an average propagation delay of 2.6 to 3.1 ns per logic decision.
2. t_{pd} measurements taken at +0.96V.

t_{pd} WAVEFORMS AT FAN-OUT = 5 PER NODE, 16" OPEN TRANSMISSION LINE



TYPICAL PROPAGATION DELAY OF AN INVERTER DRIVING 3 CASCADED AND GATES VS FAN-OUT PER NODE



FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC

CT μ L 957 DUAL-RANK FLIP-FLOP

The CT μ L 957 is a dual-rank directly-coupled Flip-Flop. The first rank or "master" consists of two cross-coupled NOR gates similar to the CT μ L 952. The second rank or "slave" employs OR ties as shown in the functional logic diagram of Fig. 1, thereby minimizing through delay. Two NAND gates provide feedback inversion, while the other two provide gating between "master" and "slave."

The primary data inputs to the Flip-Flop are through pins 1 and 7. These inputs work directly from AND gate outputs, allowing OR ties and multiple inputs to each Flip-Flop (see Fig. 2).

To take advantage of the dual-rank principle, mutually exclusive active inputs should be applied to the gating to "master" and "slave" so that only one or the other can change at any particular instant. This is easily accomplished in the CT μ L 957 due to the difference in active polarity of the two gates. Thus, what appears as a logic 1 to CT μ L gates of the Flip-Flop data inputs is a logic 0 to the "slave" gates, and vice versa.

These observations lead to the connection of pin 1 to pin 14 and pin 7 to pin 8 as shown in Fig. 2. Although both "slave" gates are not necessarily inhibited when a change takes place, the output cannot change unless both data inputs are logic 0. Therefore, this connection is the usual one, tending to minimize the loading of timing circuits.

In case phased timing signals are advantageous, pins 8 and 14 may be used independently as long as they are never active (low) while their corresponding data inputs are high.

Direct inputs to both "master" and "slave" appear on pins 2 and 6. A logic 1 (high) on either input sets or resets the "master" and simultaneously inhibits a feedback NAND gate in the "slave." The net effect is that both "master" and "slave" move to the desired condition during the presence of the direct input signal.

The response of the Flip-Flop to concurrent inputs tending to set opposite output conditions is ambiguous. That is, simultaneous logic 1 inputs must be avoided for well-defined operation.

FIG. 1. DUAL-RANK FLIP-FLOP

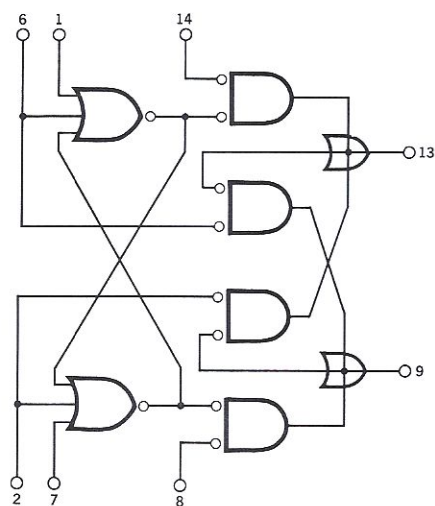
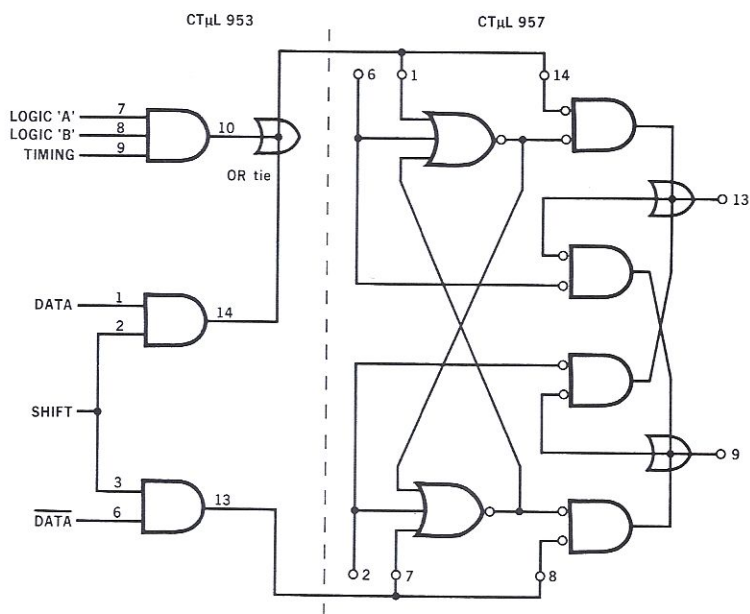


FIG. 2. TYPICAL FLIP-FLOP GATING



"OR" TIES

All CT μ L circuits have provision for output OR ties. In each of these circuits the base-emitter diode of the output transistor isolates the output from the input logic-node. Therefore, if several outputs are tied together, the output of the whole will seek the level of the most positive logic-node without disturbing the others. Along with the output emitter resistors, tied outputs are analogous with conventional diode OR circuits. An OR tie is symbolized by enclosing the tie point with a small logic OR symbol (see Fig. 2).

Each OR tie parallelstwo or more emitter resistors, reducing the total output current. Taking the fan-out capability of the lowest rated output in an OR tie as a starting point, each OR-tied output reduces the fan-out capability by one (for an N-way OR tie, fan-out capability must be reduced N-1). The most restrictive OR tie involves a Flip-Flop output, but there seems to be no practical use for such an application. OR-tied buffers lose their load factor advantage when other units are involved, so that buffers should only OR tie to other buffers.

FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC

UNCOMMITTED INPUTS

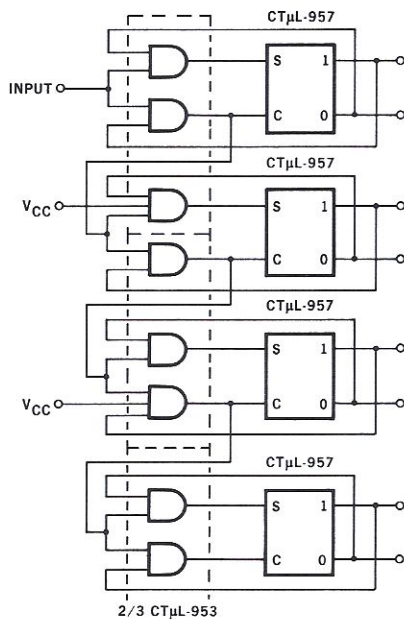
Open inputs to the CT μ L 953, 954, 955 Gates and of the CT μ L 956 Buffer are equivalent to logic zeros and effectively inhibit the device outputs. When the fan-in of these units is not fully used, spare inputs should be treated as follows:

1. CT μ L 953, 954, 955 - Return to positive supply. Parallel companion inputs to the same logic output should be avoided.
2. CT μ L 956 - Return to positive supply through 1000 Ω resistor, or connect both companion inputs to the same logic output.

PULLDOWN RESISTORS

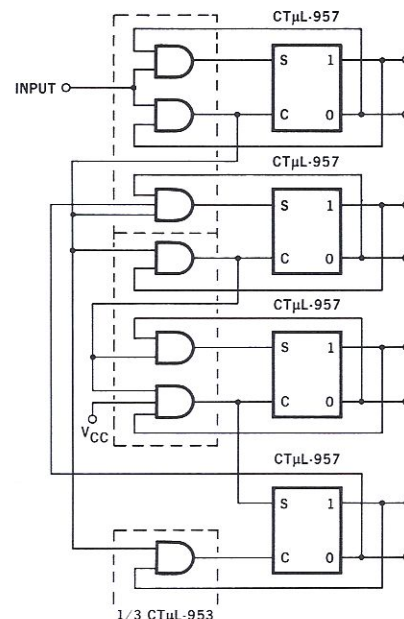
Whenever 952 Inverter Gates or 956 Buffers constitute the only loading of an output, minimum fall-time delay will not be realized unless pull-down resistors are connected to the inputs. These resistors are included in the 952 and 956 packages. One resistor suffices for each two inputs. Pull-down resistors are not needed when two or more Gate inputs or outputs are connected to the same node as a 952 or 956 input.

FIG. 3. CT μ L SERIAL BINARY COUNTER



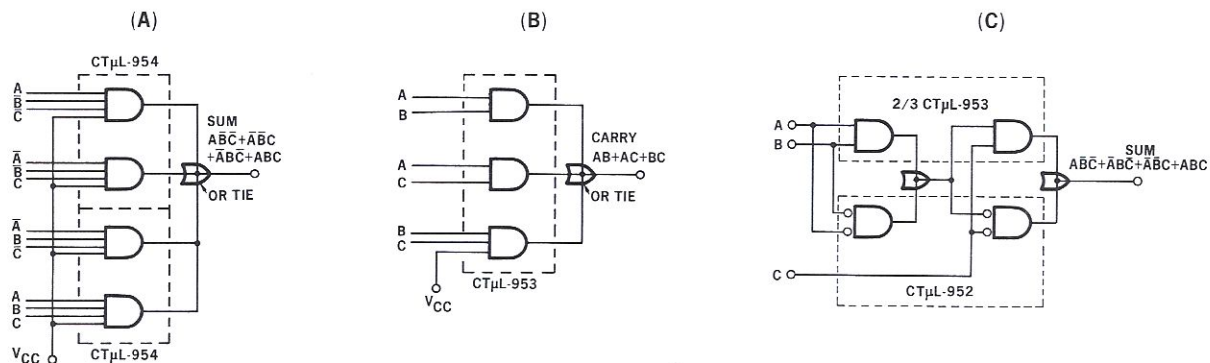
NOTES:
1. On all CT μ L-957'S, tie pins 1-14 and 7-8.
2. All gates are CT μ L-953'S.

FIG. 4. CT μ L 1-2-4-8 DECADE



NOTES:
1. On all CT μ L-957'S, tie pins 1-14 and 7-8.
2. All gates are CT μ L-953'S.

FIG. 5. HIGH-SPEED ADDER



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